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EXAMINER	
TRAN, KHANH C	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 12/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

SP

Office Action Summary	Application No.	Applicant(s)	
	10/035,567	YUAN, REBECCA	
	Examiner	Art Unit	
	Khanh Tran	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 5-28* is/are rejected.

7)☒ Claim(s) *3 and 4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The Amendment filed on 10/03/2005 has been entered. Claims 1-28 are pending in this Office action.

Response to Arguments

2. Applicant's arguments, see pages 9-17 of the Amendment, filed on 10/03/2005, with respect to the rejection(s) of claim(s) 1-3 and 5-28 under 35 U.S.C 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Andren et al. U.S. Patent 5,654,991 and Dutkiewicz et al. U.S. Patent 5,629,960.

3. The objection of claim 3 has been withdrawn after Applicant amended claim.

Claim Objections

4. Claim 4 is objected to because of the following informalities: mathematical symbol *">>"* and *"beta" are not defined in the claim*. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-2, 5-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Andren et al. U.S. Patent 5,654,991 in view of Dutkiewicz et al. U.S. Patent 5,629,960.

Regarding claim 1, in column 6 lines 15-50, figure 5 illustrates a bit sync clock adjustment circuit including an accumulator by position 42, a biggest selector 44, an adjacent sample comparator and bit sync adjust. The magnitude signal is provided to an accumulator 42 which sums the magnitudes associated with each sample position within a symbol.

Andren et al. teaches accumulating sums of the magnitudes associated with each sample position, however, does not teach accumulating a first sample sum, a first sample sum and a third sample sum as set forth in the claim.

In column 4 lines 25-35, Andren et al. expresses that in one aspect of the invention, the relationship among the early, largest and late samples can be used to adjust the bit synchronization with respect to the symbol timing of the received signal. According to figure 2, the largest corresponds to on-time sample. Because of Andren et al. suggestion, it would have been obvious for one of ordinary skill in the art at the time

the invention was made that Andren et al. teachings can be modified so that accumulator 42 accumulates sums of the early, on-time and late sample positions with respect to the symbol timing of the received signal.

Andren et al. does not teach computing the first, second and third average sample sum as set forth in the application claim.

In column 6 lines 15-48, Andren et al. teaches the accumulator sum all the first samples together, all the second samples together, etc. for a predetermined period of time. Upon the end of the selected period of time, the sums are evaluates by a biggest selector 44, which compares the accumulated sums and determines which set of samples contains the highest sum. As common knowledge of an average skill in the art, because the signal can fluctuate during the selected period of time and the fluctuation can have big effect on the accumulated sums, for that reason, it would have been obvious for one of ordinary skill in the art at the time the invention was made that Andren et al. teachings can be modified so that averaging can be performed on the accumulated sums of the early, on-time and late sample positions with respect to the symbol timing of the received signal. The biggest selector 44 performs the claimed step of identifying the maximum of the average sums. The set of samples having the biggest sum are then passed to the adjacent sample comparator 46.

Andren et al. does not teach the samples are DC compensated samples as claim in the application claim.

Dutkiewicz et al. invention is directed to a method for reducing the effects of transients on the DC offset tracking stage and the symbol timing recovery stage. In

column 3 line 25 via column 4 line 25, figure 3 discloses a system including an analog-to-digital (A/D) converter 22, a DC offset removal 22, a DC tracking stage 23, and a symbol timing recover stage 25. The DC tracking stage tracks the mean DC offset and provides a DC offset voltage 32. DC offset at baseband is often caused by a frequency offset at the receiver relative to the transmitter. As result of that, DC offset estimation is required to eliminate a residual DC signal resulting from the process of down-converting the received signal to baseband. In view of that, it would have been obvious for one of ordinary skill in the art at the time of the invention that Andren et al. teachings can be modified to implement DC offset removal and DC tracking stage as taught in Dutkiewicz et al. invention. With the modification, accumulations of the early, on-time, and late sample sums account for the computed DC offset estimate..

Regarding claim 2, the biggest sum is positive when the sample sum is positive and is otherwise of a second value.

Regarding claims 5 and 6, as recited in claim 1, the accumulator sum all the first samples together, all the second samples together, etc. for a predetermined period of time. Hence, if the maximum sum is the third sample sum, the maximum sum and the adjacent samples are then passed to an adjacent sample comparator 46 which determines the extent to which the selected biggest set of samples are centered in the peak of the received signal and whether an adjustment in the bit sync clock is desirable.

Regarding claim 7, claim 7 is rejected on the same ground as for claim 1 because of similar scope.

Regarding claim 8, as recited in claim 7, with the modification, accumulation of the early sample sum accounts for the computed DC offset estimate. The early sample sum corresponds to the claimed first set of samples.

Regarding claim 9, Dutkiewicz et al. does not teach receiving a DC offset from an initial calculator. Nevertheless, one of ordinary skill in the art would have recognized that DC tracking stage 23 provides initial DC offset estimate to DC offset removal 22.

Regarding claim 10, Andren et al. and Dutkiewicz et al. do not teach the DC offset estimate using a pilot signal. In column 6 lines 15-50, because Andren et al. suggests the period of time over which the samples are accumulated may be a portion of a preamble of the received signal, it would have been obvious for one of ordinary skill in the art at the time of the invention that Andren et al. teachings can be modified to estimate DC offset using the preamble. As common knowledge of one of ordinary skill in the art, the pilot signal is inserted in the preamble.

Regarding claim 11, as recited in claim 1, the accumulator 42 accumulates sums of the early, on-time and late sample positions with respect to the symbol timing of the received signal. In view of that, the early, on-time and late sample positions can also be

used for DC offset compensation. Hence, the early sample positions are offset by one sample with respect to the on-time sample positions.

Regarding claim 12, claim 12 is rejected on the same ground as for claim 1 because of similar scope.

Regarding claim 13, claim 13 is rejected on the same ground as for claim 12 because of similar scope. Furthermore, in column 6 lines 30-50, referring to figure 5 of Andren et al. invention, the adjacent sample comparator 46 coupled to the biggest selector 44 receives as inputs the set of samples having the biggest sum and the adjacent samples (i.e., the early and late samples) to determine the extent to which the selected biggest set of samples are centered in the peak of the received signal and whether an adjustment in the bit sync clock is desirable. If an adjustment in the bit synch clock is desirable, signals indicating that fact and the direction of the adjustment (earlier or later) may be sent to a bit synch adjust circuit 48 which adjusts the bit synch clock with respect to the received signal.

Regarding claim 14, referring to Dutkiewicz et al. invention, as recited in claim 12, in column 3 line 25 via column 4 line 25, figure 3 discloses a system including an analog-to-digital (A/D) converter 22, a DC offset removal 22, a DC tracking stage 23, and a symbol timing recover stage 25. The DC tracking stage 23 tracks the mean DC

offset and provides a DC offset voltage 32 to the DC offset removal 22, which corresponds to the claimed DC offset compensator.

Regarding claim 15, Andren et al. teachings apply to direct sequence spread spectrum receiver, which can be configured as a cellular phone.

Regarding claim 16, as appreciated by one of ordinary skill in the art, the cellular phone performs functions of a personal digital assistant, e.g. storing phone number, scheduler, etc.. Furthermore, the recitation of a new intended use for an old product does not make a claim to that old product patentable. *In re Schreiber, 44 USPQ2d 1429 (Fed. Cir. 1997).*

Regarding claim 17, as recited in claim 15, Andren et al. teachings apply to cellular phone technology. Because the receiver is part of a cellular device, the receiver can be considered as a peripheral device.

Regarding claim 18, the claimed limitations have been addressed in claim 1 rejection.

Regarding claim 19, claim 19 is rejected on the same ground as for claim 2 because of similar scope.

Regarding claim 20, claim 20 is rejected on the same ground as for claim 5 because of similar scope.

Regarding claim 21, claim 21 is rejected on the same ground as for claim 6 because of similar scope.

Regarding claim 22, claim 22 is rejected on the same ground as for claim 7 because of similar scope.

Regarding claim 23, claim 23 is rejected on the same ground as for claim 8 because of similar scope.

Regarding claim 24, claim 24 is rejected on the same ground as for claim 9 because of similar scope.

Regarding claim 25, claim 25 is rejected on the same ground as for claim 10 because of similar scope.

Regarding claim 26, claim 26 is rejected on the same ground as for claim 12 because of similar scope. Furthermore, the receiver in figure 3 of Dutkiewicz et al. invention shows an A/D converter 21, a DC tracking stage 23 connected to the A/D converter 21.

Regarding claim 27, a DC offset removal 22 is disposed intermediate the A/D converter 21 and the DC tracking stage 23. The DC offset removal 22 inherently performs initial estimation subtraction.

Regarding claim 28, claim 26 is rejected on the same ground as for claim 12 because of similar scope. Furthermore, with the combining teachings of Andren et al. and Dutkiewicz et al., DC offset removal, taught by Dutkiewicz et al., accumulator by position 42, biggest selector 44, adjacent sample comparator 46 and bit sync adjust 48 taught in Andren et al., constitute the claimed multi-hypothesis bit synchronizer.

Allowable Subject Matter

6. Claims 3-4 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kawai U.S. Patent 5,644,600 discloses "Multi-Valued Signal Decoding Circuit Having Bit Synchronization Signal Timing Transition Which Is Sampled And Held".

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Tran whose telephone number is 571-272-3007. The examiner can normally be reached on Monday - Friday from 08:00 AM - 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

kct

Khanh Cong Tran 12/23/2005

Examiner KHANH TRAN